#20/Amdt 0045
8/20/02
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Box AF
Expedited Procedure
Examining Group 2814
PATENT 740819-255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of:	)	
	)	
Hiroshige HIRANO et al.	)	Art Unit: 2814
	)	
Application No.: 09/333,049	)	Examiner: Hoai V. PHAM
	)	
Filed: June 15, 1999	)	
	)	
For: FERROELECTRIC MEMORY DEVICE	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 8/12/02
Susan Y. Shaw

AMENDMENT AFTER FINAL

Commissioner of Patents
Washington, D.C. 20231
ATTN: Box AF

Enter Marsha 10/1/02

Do not enter 8/30/02

Dear Sir:

In response to the Examiner's Final Office Action mailed February 13, 2002, please consider the following amendments and remarks in connection with the above-identified application.

IN THE CLAIMS:

✓ ✓ ✓ ✓

Please amend claims 1, 6, 8 and 9 as follows:

1. (Four Times Amended) A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

E1